Electronic Version
Stylesheet Version v1.1.1

Description

SYSTEM AND METHOD FOR IMPLEMENTING SELF-TIMED DECODED DATA PATHS IN INTEGRATED CIRCUITS

BACKGROUND OF INVENTION

[0001] The present invention relates generally to data transmission paths for integrated circuit devices and, more particularly, to a system and method for implementing self-timed, decoded data paths for input/outputs systems in integrated circuits.

[0002] Digital data paths for wide input/output (I/O) circuits and macros in integrated circuit devices typically consume the largest percentage of power within the macro and are often in the critical performance path. This in turn drives a desire to reduce the power consumption of the data path while maintaining the same performance level. In order to properly size power supplies for such wide I/O devices, "worst case" data patterns are assumed. In the context of digital data I/O devices, this worst case is represented by

the data for each path changing on each clock cycle, since this results in charging/discharging of the data lines that define each data path.

[0003] Relatively speaking, single ended static systems (i.e., those systems in which only the true value of the digital bit, and not the complement thereof, is transmitted on a data line, and which line is not precharged to a defined value) consume the least amount of worst case power for full rail designs, because power is only consumed every other clock cycle. However, with a single ended data bus (either static or dynamic), the latching of the received data is not "self-timed" because the complementary bit is not transmitted to the receiving latch, and thus the data capture is dependent upon a global strobe (i.e., system clock). This is also the case for a single ended dynamic system, where a single true leg is pre-charged to a logic "1" state and discharged only when transmitting a logic "0" state. Self-timing cannot be performed because a transition is not guaranteed on each data bit independent of its state. Other low power data paths utilize small signal swing data lines with local amplification, but again this comes at the expense of performance, complexity and potential noise issues.

[0004] On the other hand, dynamic precharge schemes utilize data lines for both the true bit and its complement. In operation, the true/complement data line pairs are precharged to a known state, and one is thereafter discharged during data transmission. This configuration offers better performance as a result of the self-timing capability, given that the dual lines provide either a set or a reset signal to the capture latch. Therefore, the time lost in using a global strobe or clock that must satisfy reasonable data setup times to the capture latch is removed. The capture latch will transition to the new data state as soon as the data is available. Conversely, this scheme consumes twice the power of the single ended static system, since one data line always switches during each cycle in the worst case power consumption scenario.

[0005] Accordingly, it would be desirable to be able to minimize the power consumption of such data lines while still providing the benefits of self-timing.

SUMMARY OF INVENTION

[0006] The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a self-timed data transmission system. In an exemplary embodiment, the system includes a data bit group defined by at least

two data bits to be transmitted from a corresponding plurality of transmitting storage elements. A corresponding plurality of data receiving storage elements receives the data transmitted from said transmitting storage elements. Encoding logic is used for encoding the transmitted data from the transmitting storage elements, wherein the encoded transmitted data is coupled to a plurality of data lines. The encoding logic is further configured so as to result in only one of the plurality of data lines being activated during a given data transmission cycle.

[0007] In another aspect, a self-timed, digital data input/output (I/O) path transmission system includes a data bit group defined by at least two data bits to be transmitted from a corresponding plurality of transmitting latches. A corresponding plurality of data receiving storage latches receives the data transmitted from the transmitting latches. Encoding logic is used for encoding the transmitted data from the transmitting latches, wherein the encoded transmitted data is coupled to a plurality of data lines. In addition, decoding logic is used for decoding the encoded transmitted data on the plurality of data lines, the decoding logic being coupled to the receiving latches. The encoding logic is further configured so as to result in only

one of the plurality of data lines being activated during a given data transmission cycle.

[0008] In still another aspect, a method for transmitting self-timed data within a multiple input/output (I/O) data path includes configuring the data path into data bit groups defined by at least two data bits to be transmitted from a corresponding plurality of transmitting storage elements. The data to be from the transmitting storage elements is encoded and coupled onto a plurality of data lines, and the data from the plurality of data lines is then decoded. The decoded data is thereafter received by a corresponding plurality of data receiving storage elements. The encoding of the data is implemented in a manner so as to result in only one of the plurality of data lines being activated during a given data transmission cycle.

BRIEF DESCRIPTION OF DRAWINGS

[0009] Referring to the exemplary drawings wherein like elements are numbered alike in the several Figures: Figure 1 is a schematic diagram of an existing, single ended, static data bus for a pair of data bits; Figure 2 is a schematic diagram of an existing, double ended true/complement data bus for another pair of data bits;Figure 3 is a schematic diagram of a grouped, encoded data path lay-

out for a pair of data bits, in accordance with an embodiment of the invention; Figure 4 is a truth table illustrating the operation of the encoding/decoding logic of the self-timed data bus system depicted in the embodiment of Figure 3; and Figure 5 is a timing diagram comparing the data transferring operations of the systems of Figures 1-3.

DETAILED DESCRIPTION

[0010] Disclosed herein is a system and method for implementing self-timed, decoded data paths that consume less power than conventional self-time data path systems. Briefly stated, at least a pair of data bits are "grouped together" through logic encoding and decoding circuitry such that, within a given group, only one line in the group is activated during transmission of the grouped data bit information. As such, the line that activates represents a decoded state for the whole group. In this manner, power consumption is substantially reduced, while still maintaining the high performance of a self-timed data receiving latch.

[0011] Referring initially to Figure 1, there is shown a schematic diagram of an existing, single ended, static data bus system 100 for a pair of data bits. More specifically, a pair of

transmitting data latches L0, L1 are coupled to a corresponding pair of data receiving latches, D0, D1, through data lines 102, 104 (as well as buffers B0, B1, respectively). As stated previously, in this single ended configuration, only the true node of each latch L0, L1 is coupled to the input (D) of each data receive latch D0, D1. Accordingly, a clock input (CLK) is used to latch the data to the outputs Out 0, Out 1. The design of a sufficient setup time for the latch clock becomes increasingly problematic with a large number of I/O data paths since longer setup time delays data access. Also, overly aggressive setup times can result in failure to latch the correct data, a problem that self timing completely avoids.

[0012] In contrast, Figure 2 is a schematic diagram of an existing true/complement data bus system 200 featuring another pair of transmitting data latches L2, L3, each coupled by a pair of data lines to corresponding data receive latches, D2, D3. In this double ended, true/complement configuration, both the true and complement nodes of latches L2, L3 are coupled to latches D2, D3 through a total of four data lines, 202, 204, 206 and 208. Figure 2 also illustrates the use of clock signal CLK to trigger the data transmit operation of the true and complement nodes by

NAND gates 210 and buffers 212. In addition, the receive latches D2, D3 are S-R (SET/RESET) latches depicted schematically by a pair of cross-coupled NAND gates 214, as will be recognized by one skilled in the art. Furthermore, although a ground precharge, V_{dd} active system is presumed in Figure 2, it will be appreciated that a V_{dd} precharge, ground active design could be used as well.

[0013] The true/complement system 200 of Figure 2 illustrates how the true and complement data bit pairs are used to directly control the set and reset of the capture latch. Specifically, the data transitions either on the true or complement leg act to directly set or reset the latch. In this scheme, each data bit self-times its respective data receive latch, thereby removing the need for clock generation and data setup to clock. Whereas the single ended static system 100 requires that a high to low transition and a low to high transition be equally as fast, the true/complement system 200 only requires that one of the two transition types to be quick (since only one transition is in the access path, while the other is in the restore path). This in turn allows for optimization of the "forward path" at the expense of the "reverse path", leading to smaller device area for the restore devices and faster operation of

the forward path.

[0014] As stated previously, however, the true/complement system 200 of Figure 2 also consumes twice the power of the single ended, static system 100 of Figure 1. Therefore, in accordance with an embodiment of the invention, there is disclosed a self-timed, decoded data path system in which at least two data bits are "grouped" by encoding logic such that the transmission of data therefrom results on only one data line being discharged during a given clock cycle.

[0015] Referring now to Figure 3, there is shown a schematic diagram of one possible embodiment of the self-timed, decoded data path system 300. For purposes of comparison, Figure 3 also illustrates the transmission of data between a pair of data transmission latches L4, L5 and a corresponding pair of data receiving latches D4, D5, over data lines 302, 304, 306, 308. As was the case in Figure 2, the data receiving latches D4, D5 are depicted as S-R latches. In order to reduce consumed power, the data bit information for both L4 and L5 is grouped together for transmission purposes by encoding logic 310 and decoding logic 312. In other words, instead of two independent data bits each having a pair of data lines associated therewith, the

data bit information originating from L4 and L5 is encoded and transmitted using a set of four data lines.

[0016] The encoding of the data is implemented through encoding logic 310 such that only one of the four lines 302, 304, 306 and 308 will "fire" (e.g., be discharged to ground) during a transmission cycle, regardless of the particular value of the true data bits for L4 and L5. Correspondingly, the discharge to ground of one of the four lines 302, 304, 306 and 308, combined with decoding logic 312, will cause either a SET or a RESET operation in D4 and D5 so as to store the properly decoded data bits therein. It should be understood that the encoding/decoding logic shown in Figure 3 is only an exemplary logical representation of the operations carried out by the system, and not necessarily the actual circuits used. One skilled in the art will recognize that the actual logic functions may be carried out by any number of possible logic gate configurations. Moreover, the design of the latches and data drive buffers may be optimized for each specific implementation to provide the best performance.

[0017] The added delay of any AND/OR gates associated with the logic can be almost completely removed from the system with proper design. For example, an AND/NAND gate may

be integrated into a buffer design such that the total delay is very close or identical to the single input buffer of the T/C system. Also, with regard to the capture latches, providing two parallel SET inputs and two parallel RESET inputs (as shown schematically in Figure 3) can remove the need for any OR logic that would otherwise slow down the data path. For designs that have multiple drive locations on a single bus, converting the buffer logic to tri-state buffer logic will allow for "dotting" multiple decode drivers on a single decode bus. Many T/C data latches for memories utilize precharge logic that holds both the true and complement latch outputs at the same state (ground precharge for example). This third data state can be used to tri-state the buffer.

[0018] Figure 4 is a truth table that further illustrates the operation of the encoding logic 310 and decoding logic 312. As is shown, when the value of the data bits from L4 and L5 are both logic "0", only data line 308 will be discharged to ground upon the activation of the transmit clock, since only the NAND gate coupled to line 308 has its output at logic "0". At the decoding logic end, discharged data line 308 causes a SET operation at both D4 and D5, which results in the correct latching of a "0" bit in each. When L4

transmits a "1" and L5 transmits a "0", only data line 306 is discharged, causing a RESET operation and D4 and a SET operation at D5. When L4 transmits a "0" and L5 transmits a "1", only data line 304 is discharged, causing a SET operation at D4 and a RESET operation at D5. Lastly, whenever both L4 and L5 transmit a "1", only data line 302 is discharged, causing a RESET operation at both D4 and D5.

[0019] Figure 5 is a timing diagram 500 that provides a comparison of the data transfer operation of each of the conventional schemes of Figures 1 and 2 with the present invention embodiment of Figure 3. The top portion of the timing diagram 500 illustrates that the data transmitted from each pair of transmitting latches from the three respective systems is the same over four clock cycles for comparison purposes. The output data shown at the bottom of diagram 500 (i.e., the data received by the receiving latch pairs) is also the same for each system 100, 200, 300.

[0020] The difference between the data transmission and power consumption in the three systems is reflected in the highlighted portion 502 of the timing diagram 500. In the single ended system 100, the least amount of power is consumed as reflected by the transition in the potential on

lines 102 and 104. Again, the primary disadvantage of this configuration is the reliance on the system clock to latch the captured data. In the true/complement system 200 (where all lines are precharged to high), it will be seen that during each clock cycle, one of the true or complement lines for both bits are always discharged.

[0021] More specifically, Figure 5 shows that during the transmission of (0, 0) at the first clock cycle, complement lines 204 and 208 are discharged. At the second clock cycle, the transmission of (0, 1) results in true line 202 of L2 and complement line 208 of L3 being discharged; at the third clock cycle, the transmission of (1, 0) results in complement line 204 of L2 and true line 206 of L3 being discharged; and at the fourth clock cycle, the transmission of (1, 1) results in true lines 202 and 206 being discharged. In contrast, for the system 300 of the present disclosure, during the same four clock cycles, only one of the four total lines (302, 304, 306, 308) is discharged.

[0022] Although the embodiment of Figure 3 depicts a system 300 in which two data bits are used in an encoded group, it will be appreciated that more than two data bits may also be grouped together in this manner. It therefore follows that the larger the grouping of the data bits, the less

power is consumed. Table 1 below provides a comparison of data group size, associated wiring and power consumption.

[0023] **Table 1: Data Group Size, Wiring, and Power Comparison**

Number of Data bits in Group	T/C Pairs	Decoded Lines	Power
1	2	2	1 x
2	4	4	0.5 x
3	6	8	0.33 x
4	8	16	0.25 x

[0024] As can be seen from the above table, with no grouping of data bits per se (i.e., 1 bit per "group"), there are a total of two true/complement data lines, and thus two "decoded" lines used in the transmission of the data, as was described in Figure 2. The power consumption associated with this configuration is normalized to a value of 1 (full power) for comparison purposes. If, however, a group of two data bits is created for transmission purposes, there are now four total data lines in the group (two true lines, and two complement lines). This is the embodiment depicted in Figure 3. In order to encode a two-bit segment of data, wherein only one line represents each of the possible data combinations, a total of 2^2, or four decoded

lines are needed. Since there are a total of four lines already associated with two, true/complement pairs, no additional wiring is needed for carrying out the encoding/decoding function. As was also discussed earlier, the discharging of only one of four data lines represents a 50% power savings (equivalent power to the single ended system)If the group were to be expanded to include three bits, then only one of 2^3, or eight decoding lines has to be discharged during the three-bit transmission. This would then represent a power consumption of only 33% with respect to the true/complement scheme. However, since a three-bit latch group only has a total of six T/C lines available, an additional two lines are needed for the encoding function. As a result, the issue of using additional chip real estate now comes into consideration. This becomes even more apparent as the group size is increased; an n-bit group requires 2^n decoding lines, but only 2n T/C lines are conventionally available.

[0025] Accordingly, because a group of two data lines uses the same amount of wiring as a true/complement system and uses only half of the power thereof, it is the preferred embodiment for a self-timing data path. Additional power savings by increasing the bit group size would then result

in an exponential tradeoff in additional area needed for the decoding lines.

[0026] As will be appreciated, the above described self-timed, decoded data path configuration may be utilized in conjunction with a wide variety of applications such as address busses, content addressable memories (CAM), DRAM, SRAM, microprocessors, application specific integrated circuits (ASIC), etc. Many high-speed memories, for example, use true/complement address busses that are precharged at the end of each cycle. Thus, converting these address paths to decoded address paths versus straight T/C transmission can reduce power consumption while maintaining performance and self-timing.

[0027] While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best

mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.